

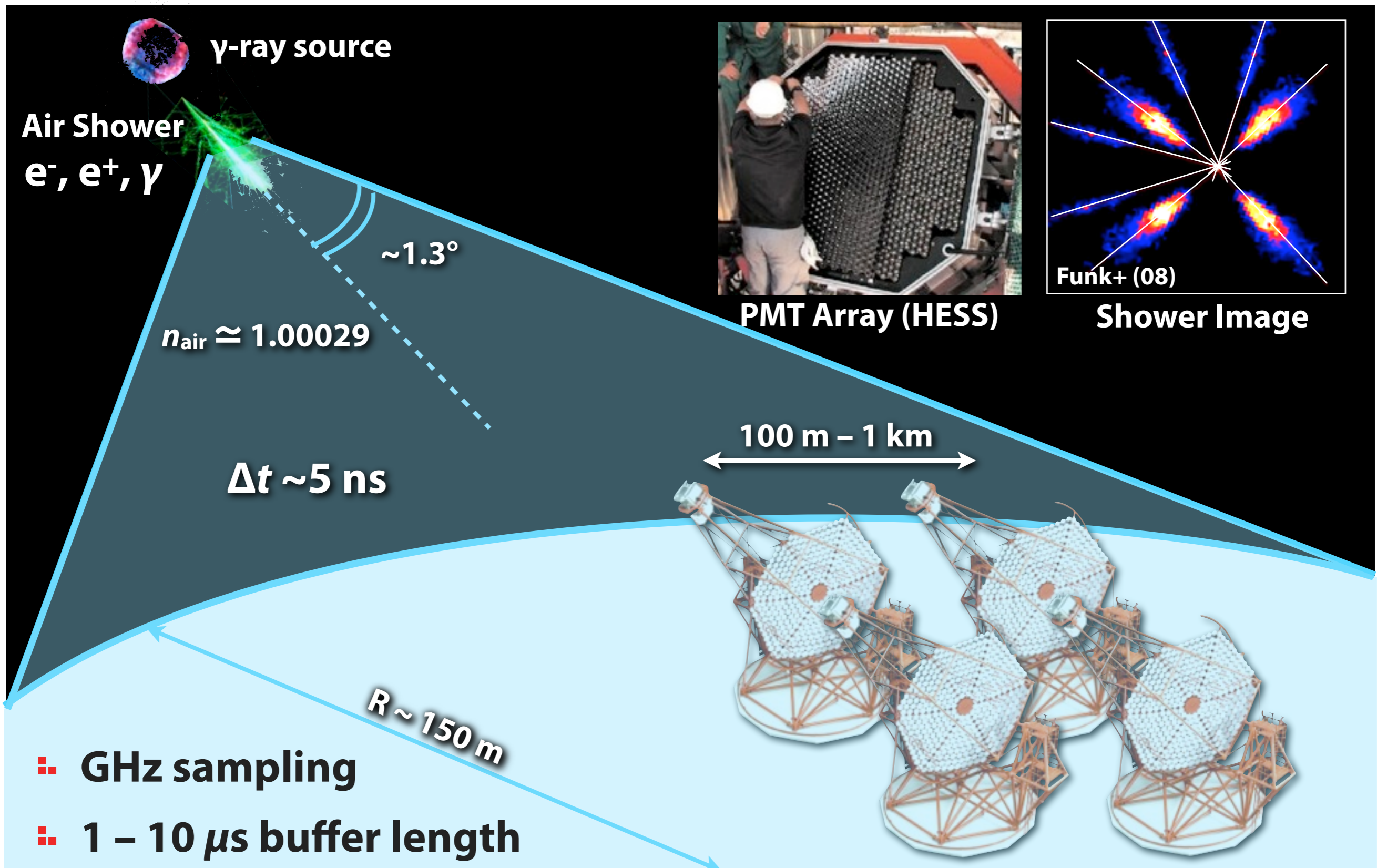
CTA デュアルミラー光学系用の 1 GHz 波形記録回路 TARGET の開発と性能評価

奥村 暁^A、田島 宏康^A、日高 直哉^A、K. Bechtol^B、S. Funk^B、L. L. Ruckman^C
A. Simons^B、J. Vandenbroucke^B、G. Varner^C
for the CTA Consortium

名大 STE 研^A、SLAC^B、ハワイ大^C

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Detection Technique for 10 GeV to 100 TeV Gamma Rays



The Cherenkov Telescope Array (CTA) Observatory

LST × 3–5
 $D \sim 23$ m
FOV $\sim 4\text{--}5^\circ$
Pix $\sim 0.1^\circ$
 $E \sim 0.02\text{--}5$ TeV

MST × 15–25
 $D \sim 12$ m
FOV $\sim 7\text{--}8^\circ$
Pix $\sim 0.18^\circ$
 $E \sim 0.1\text{--}30$ TeV

SC-MST × 36
 $D = 9$ m
FOV = 8°
Pix = 0.07°
 $E \sim 0.1\text{--}10$ TeV

SST × 25–100
 $D \sim 4\text{--}7$ m
FOV $\sim 7\text{--}10^\circ$
Pix $\sim 0.2\text{--}0.25^\circ$
 $E \sim 1\text{--}300$ TeV

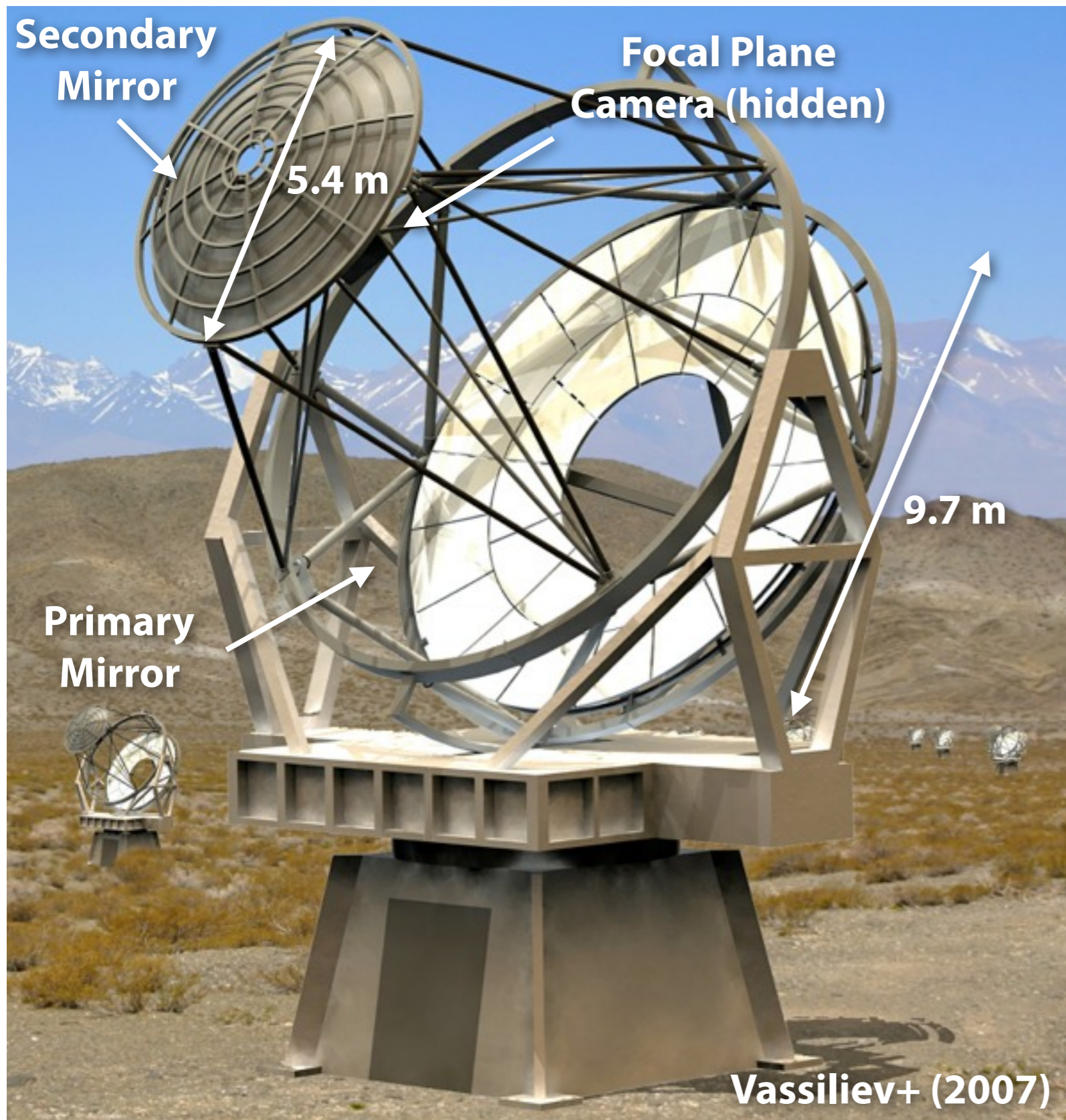
Dual Mirror

Dual Mirror ?



- ❖ The next-generation gamma-ray Cherenkov telescope
- ❖ Consists of Large/Medium/Small Size Telescopes (**LSTs/MSTs/SSTs**)
- ❖ + Extension using **Schwarzschild-Couder MSTs** proposed by CTA-US + Nagoya

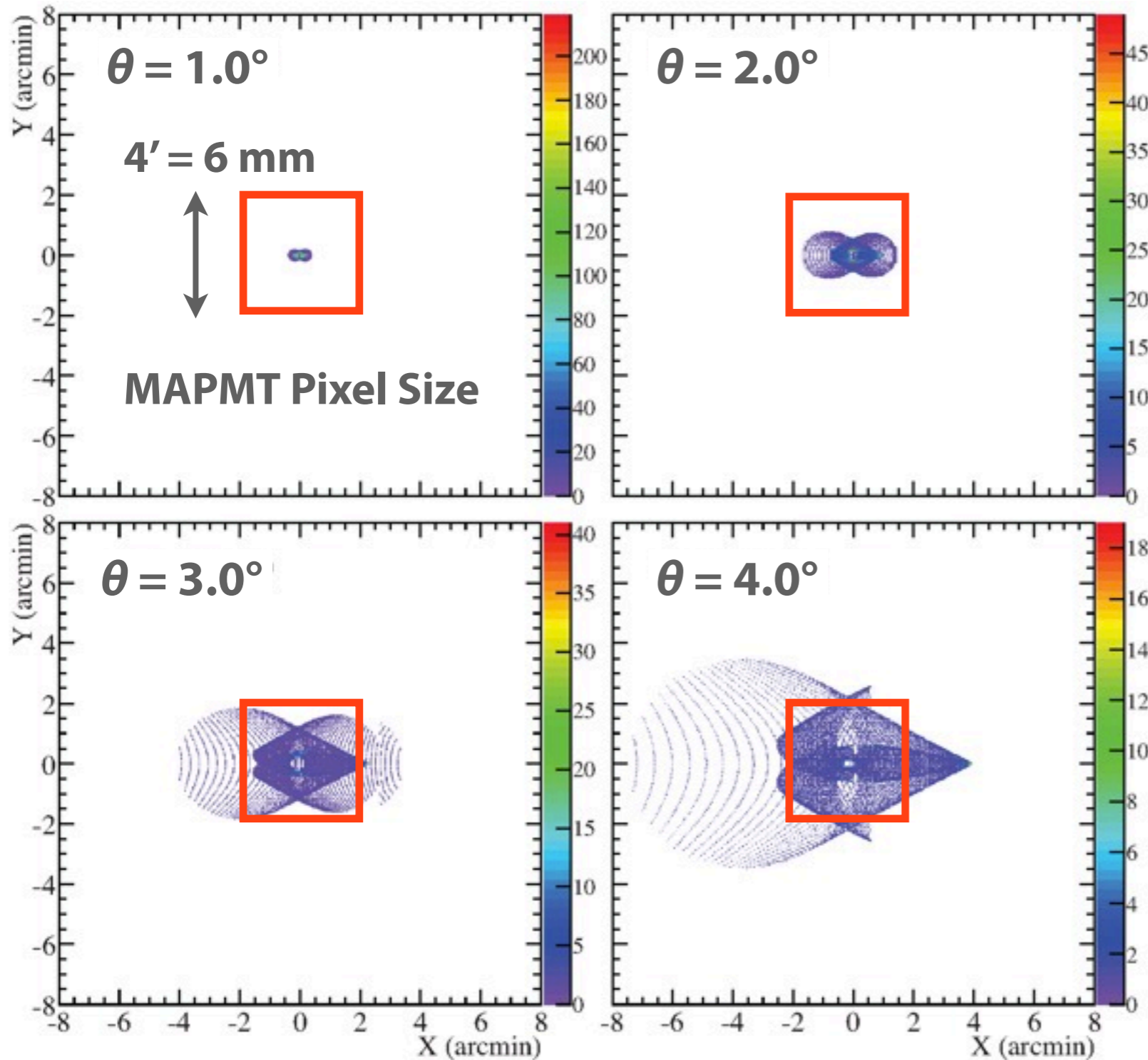
The Schwarzschild-Couder Optical System



- ❖ The first challenge of a **dual-mirror system** in CR experiments
- ❖ **9.7-m** primary + **5.4-m** secondary
- ❖ Wide FOV of **8°**
- ❖ Small spot size of **< 6 mm (4 arcmin)**
- ❖ MAPMT array consisting of more than **11,000 channels**

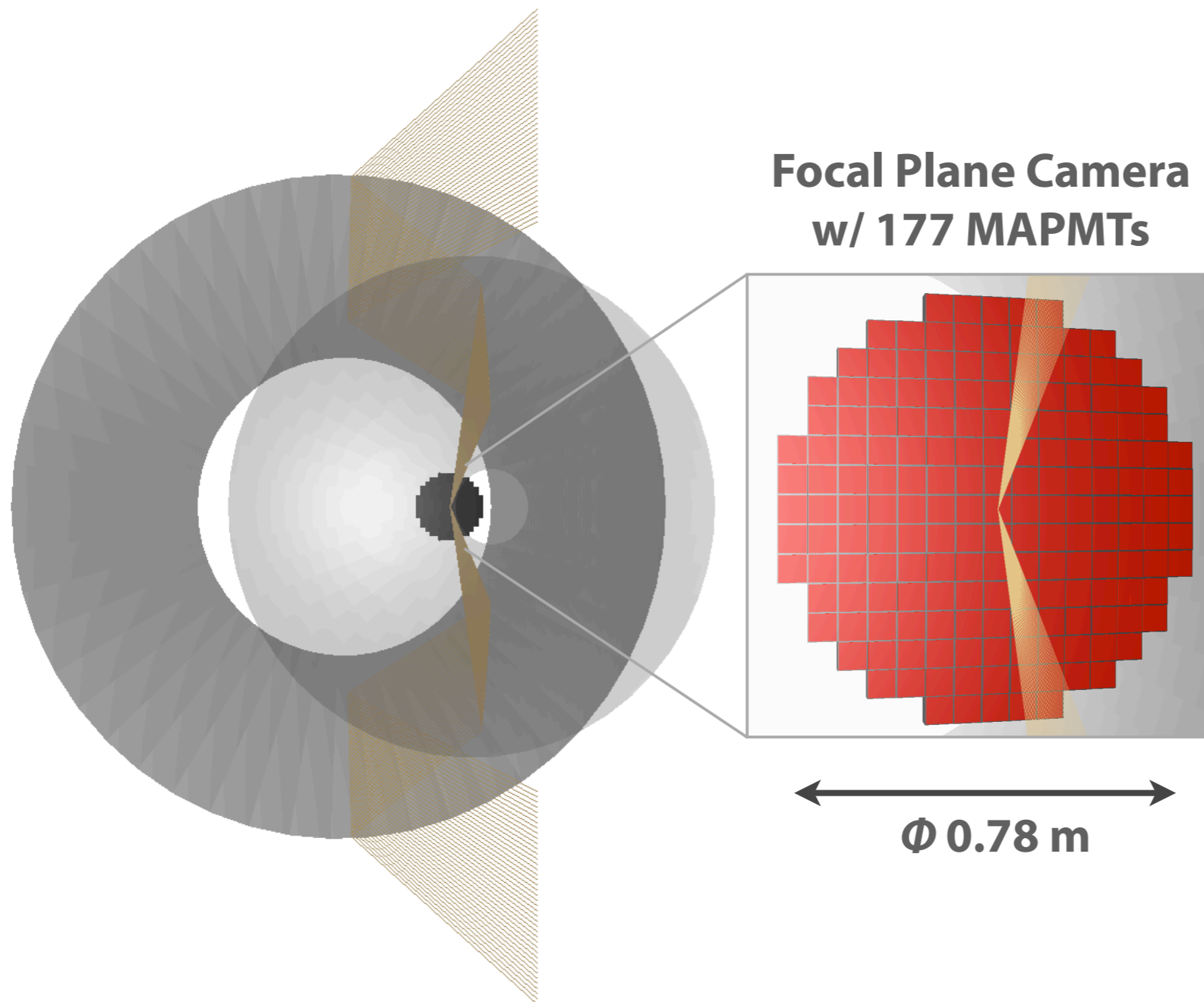
The Schwarzschild-Coude Optical System

Spot Diagrams



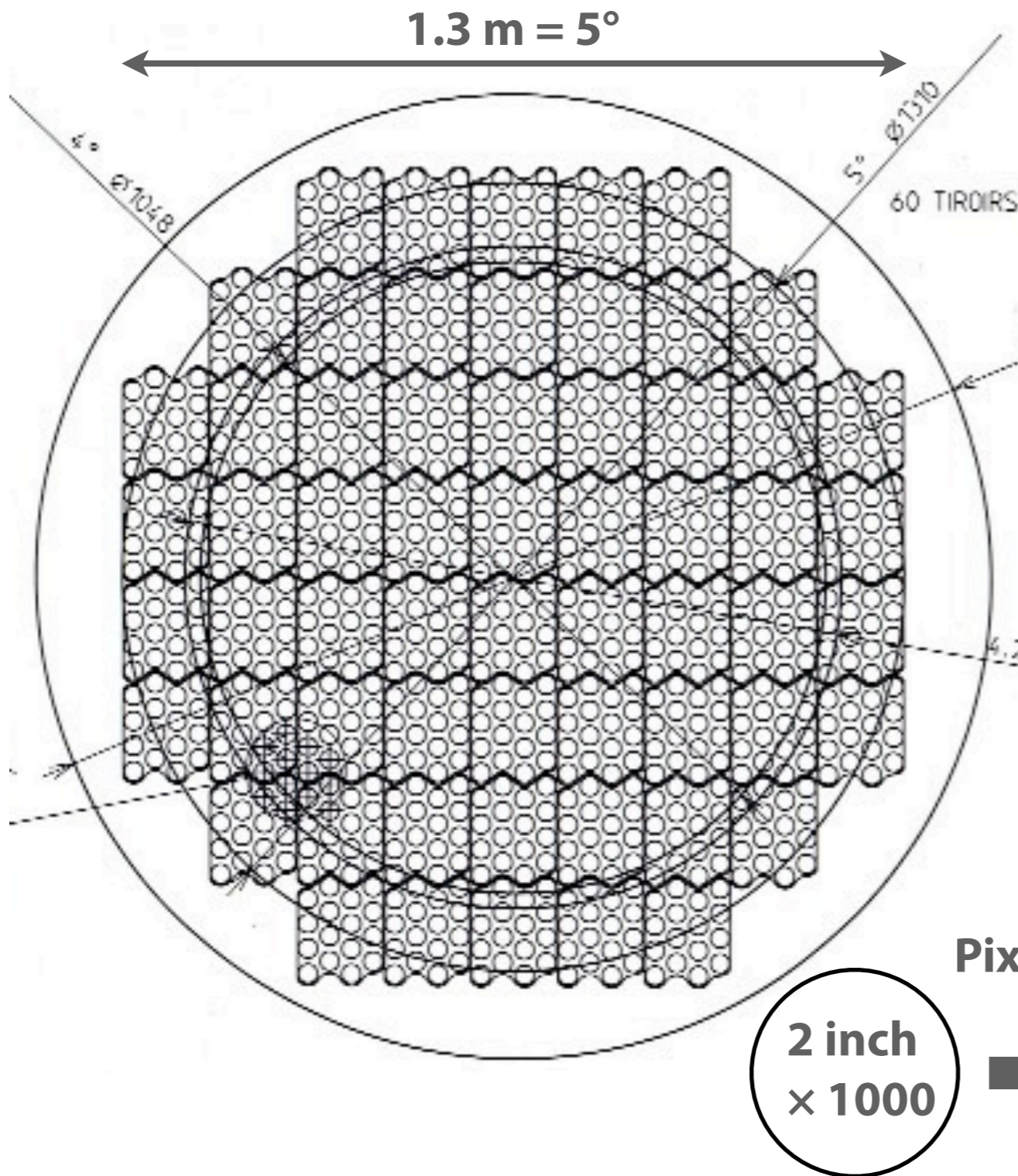
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The Schwarzschild-Coude Optical System

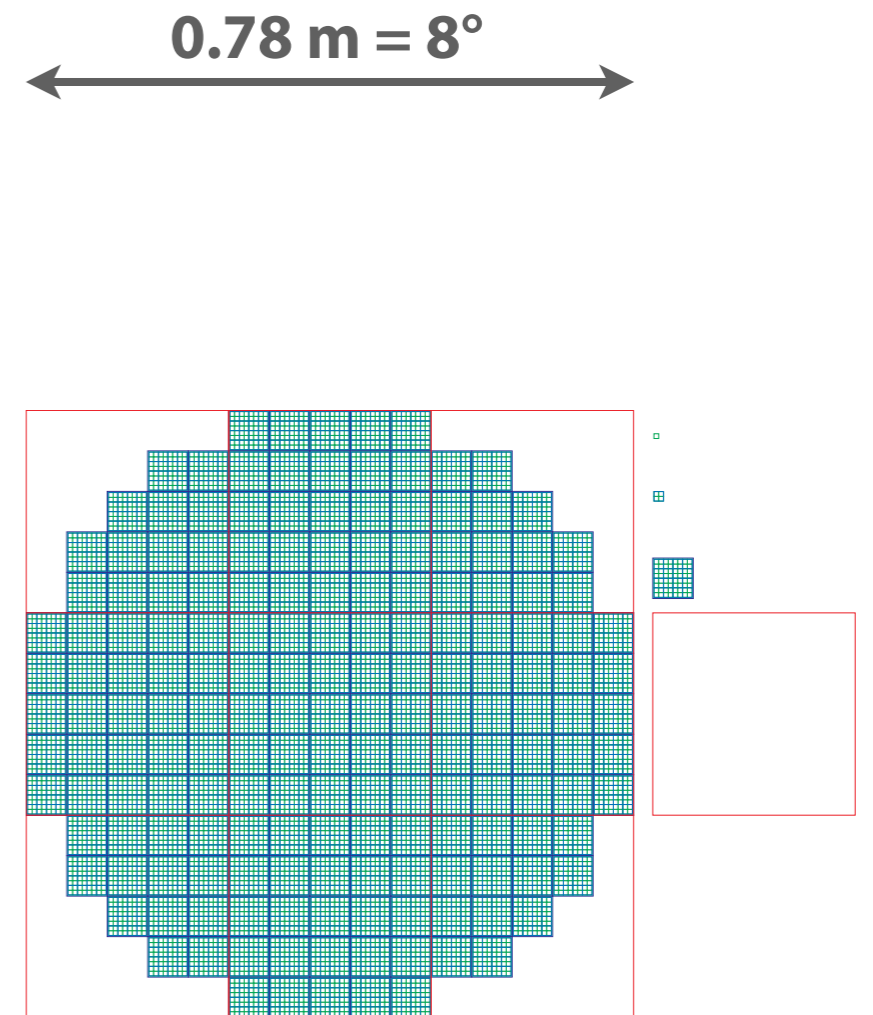


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Need a Very Compact Front-end Electronics with Low \$/ch



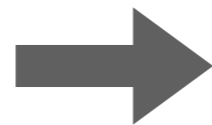
HESS Camera w/ Regular PMTs



SC Optics Camera w/ MAPMTs or MPPCs

Pixel Size

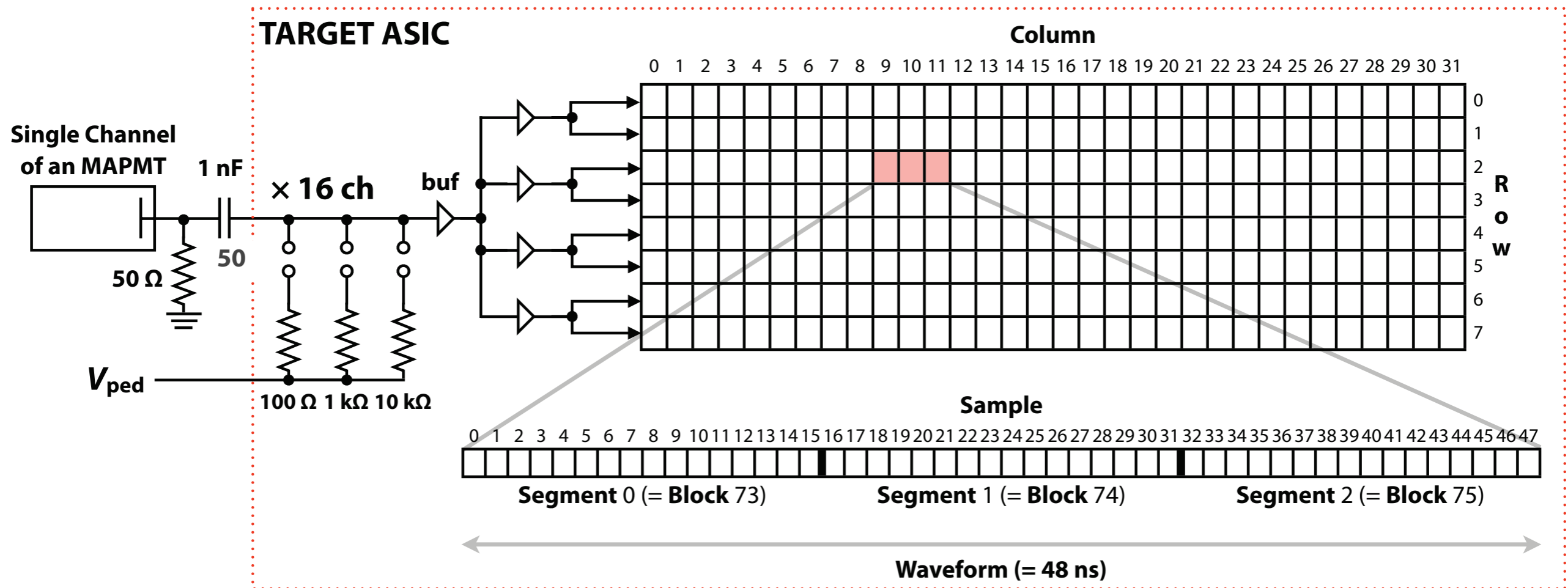
2 inch
× 1000



6 mm
× 10000

TARGET-1 Concept

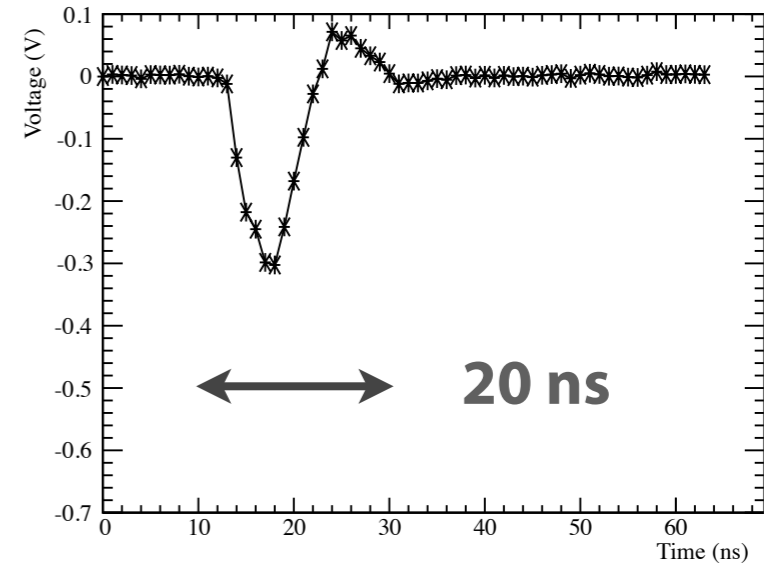
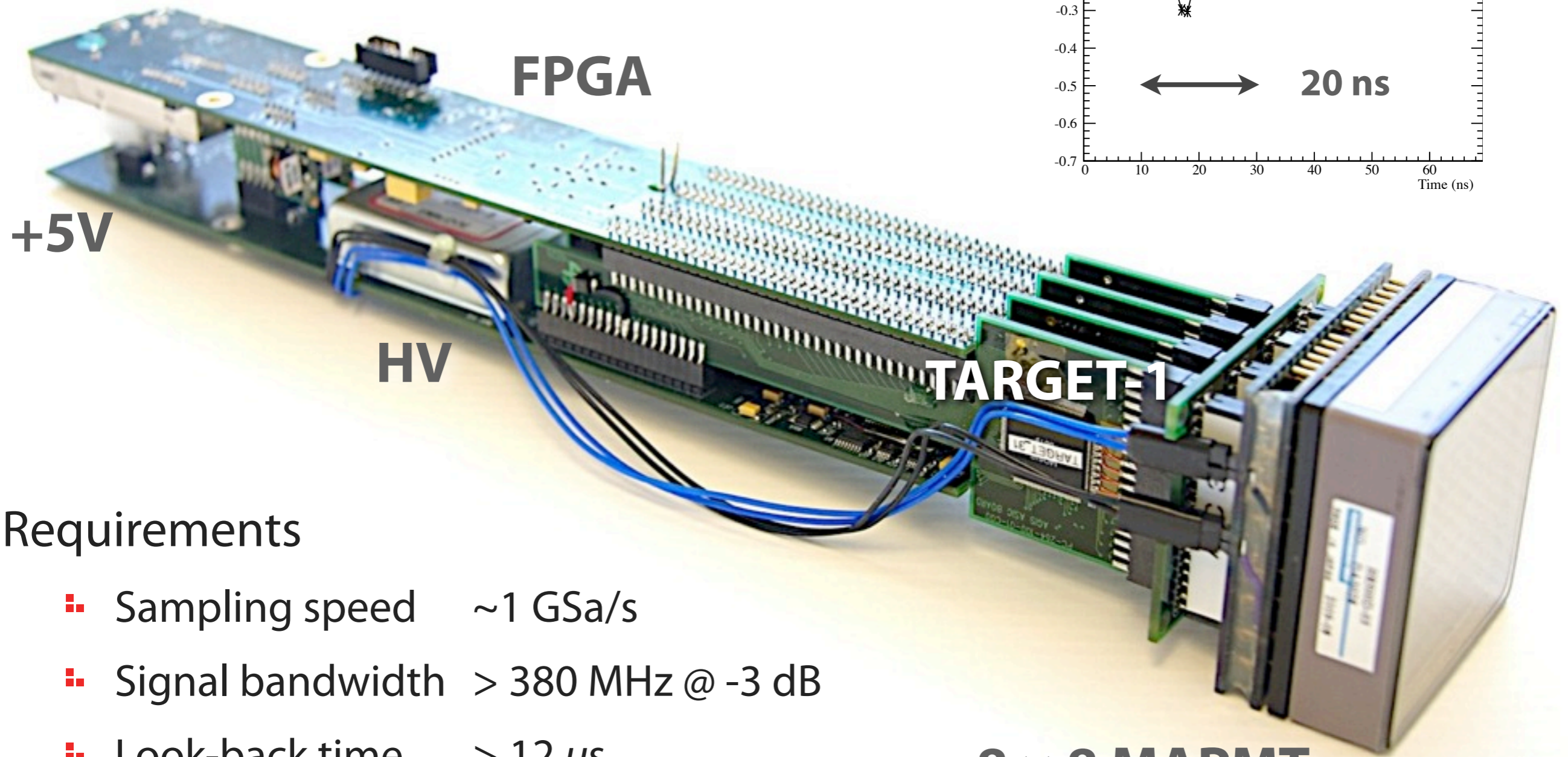
TARGET = TeV Array with Gsa/s sampling and Experimental Trigger



- ❖ **16-ch** integrated system × **4096 capacitors** (= 4- μ s buffer at 1 GHz)
- ❖ **1 GHz or faster** sampling speed, **self trigger**
- ❖ **9 or 10-bits** dynamic range, digitized by Wilkinson-type ADCs
- ❖ Low cost (~**\$20/ch**), low power (~**5W/64ch**)

The TARGET-1 ASIC + Camera Module

Fiber USB



Requirements

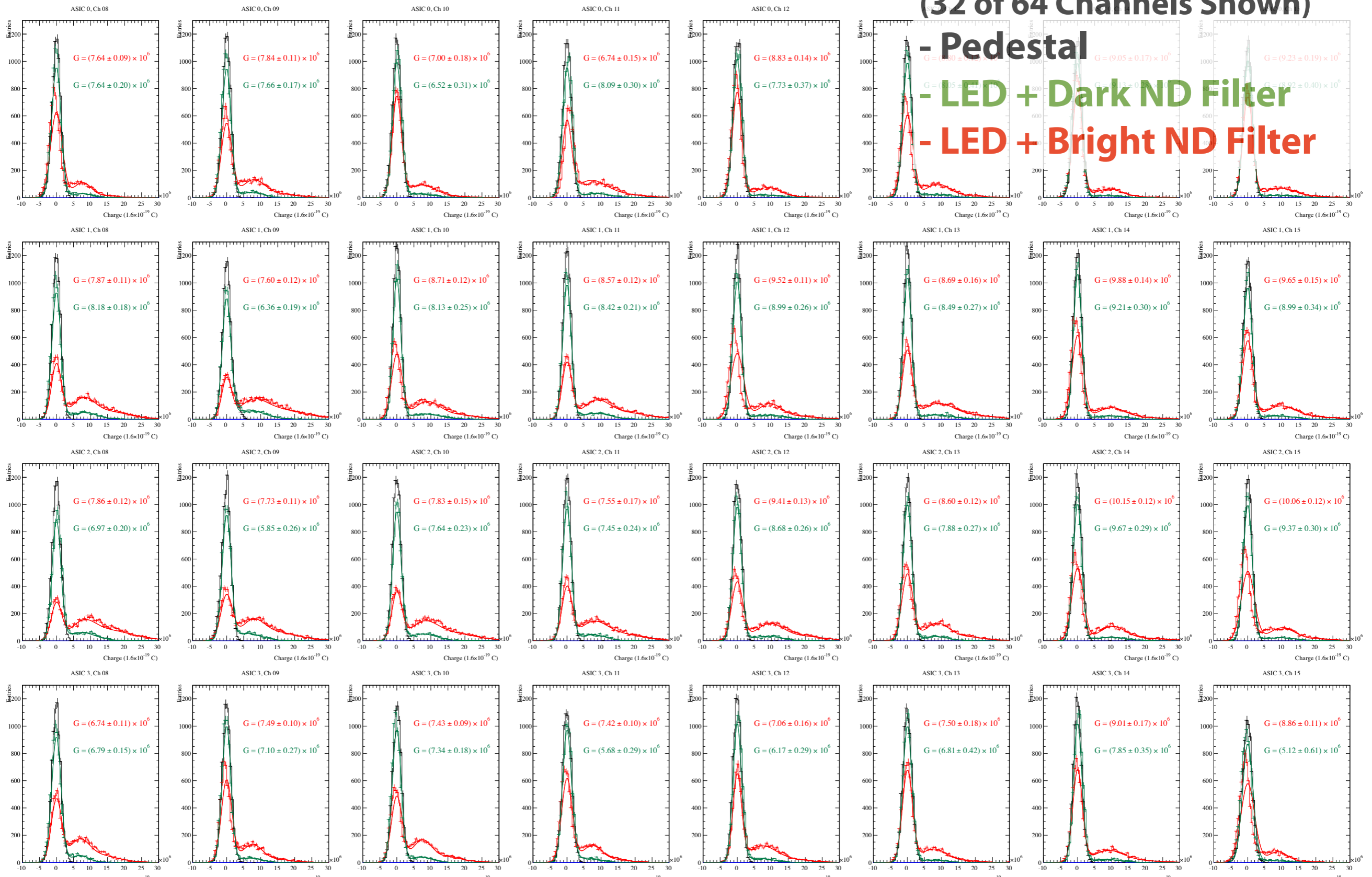
- ❑ Sampling speed ~ 1 GSa/s
- ❑ Signal bandwidth > 380 MHz @ -3 dB
- ❑ Look-back time $> 12 \mu\text{s}$
- ❑ Dynamic range > 9 bits

**8 × 8 MAPMT
(H8500D-03)**

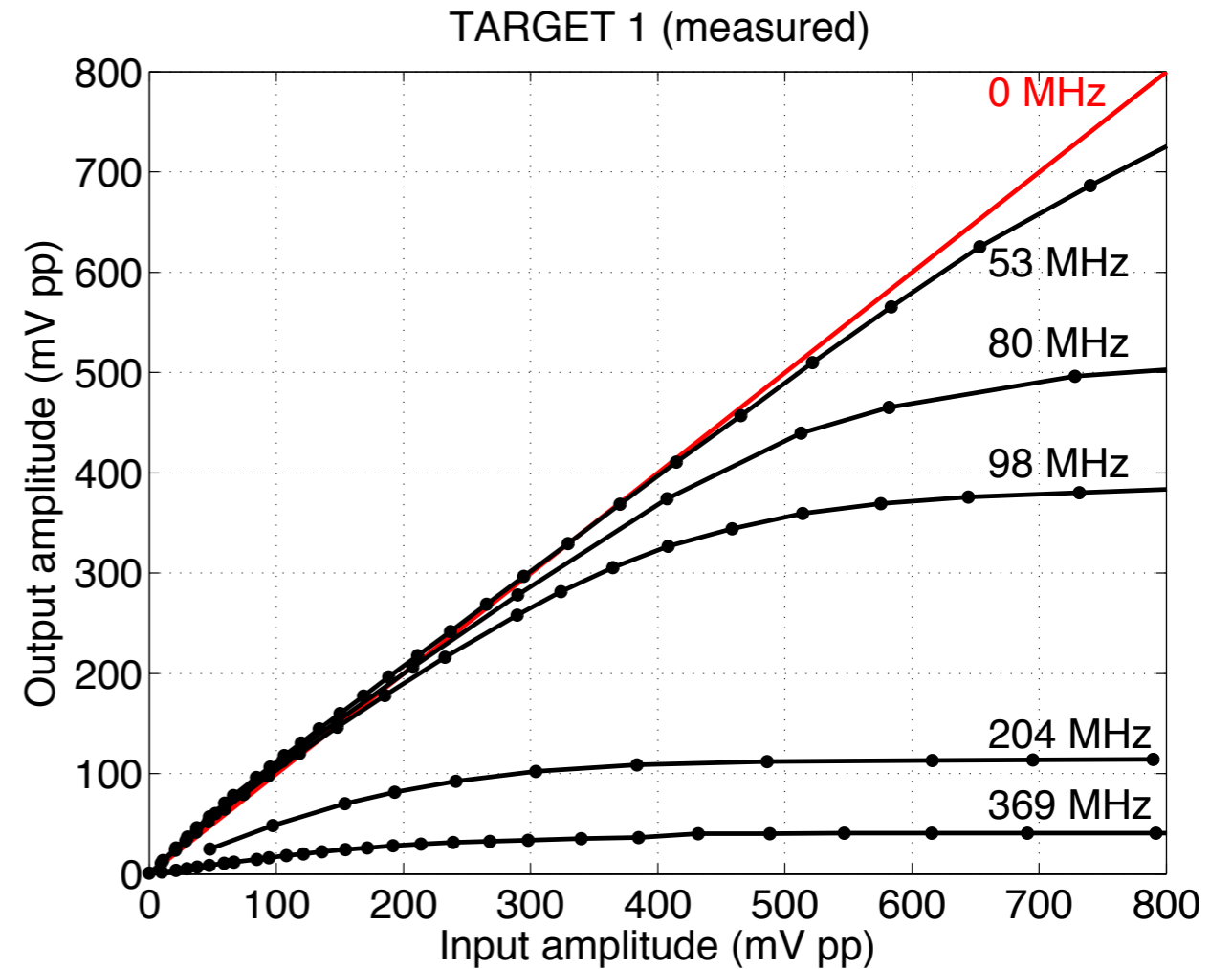
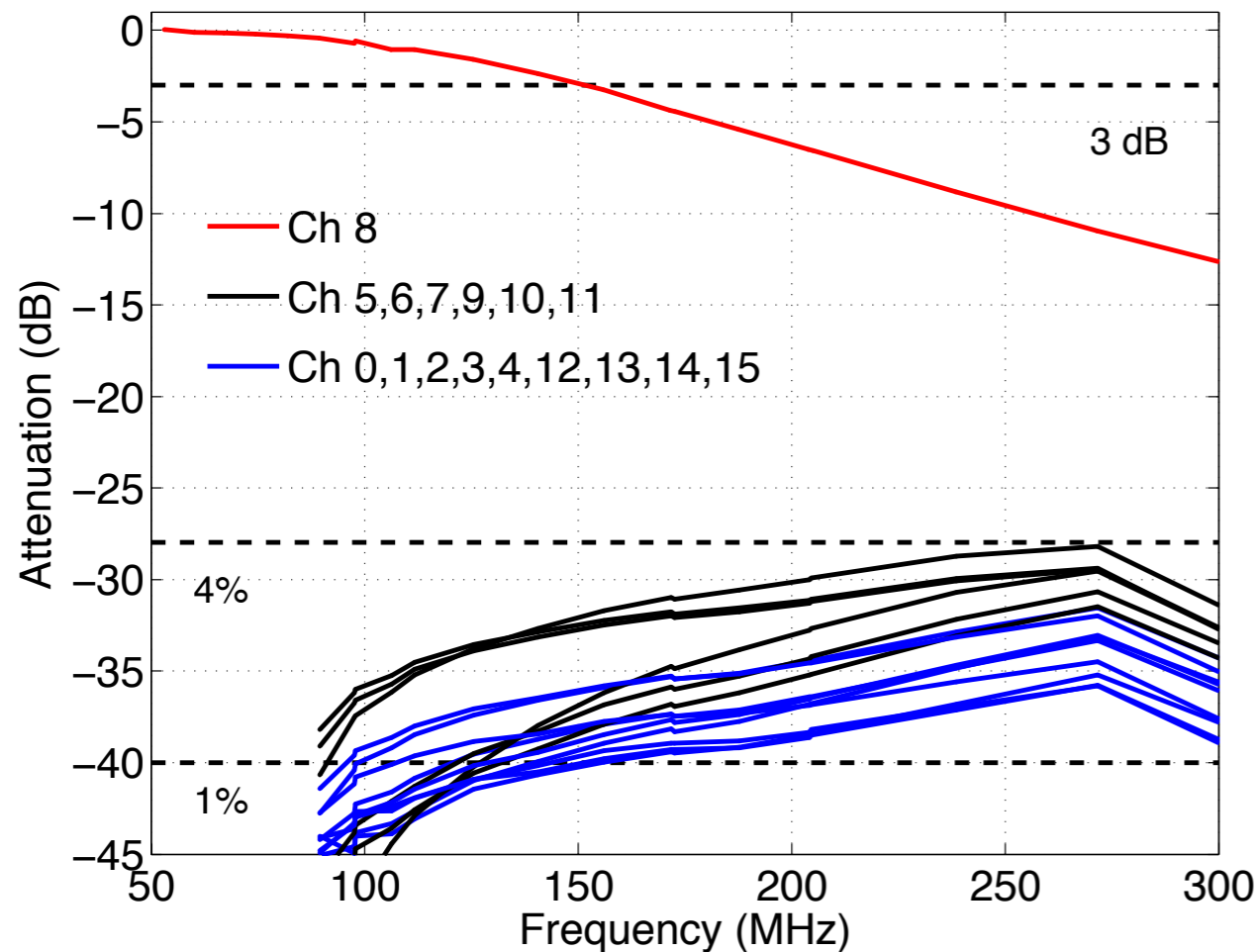
Performance Tests of TARGET 1 (1 p.e. Distribution)

(32 of 64 Channels Shown)

- Pedestal
- LED + Dark ND Filter
- LED + Bright ND Filter



Performance Tests of TARGET 1 (Bandwidth)



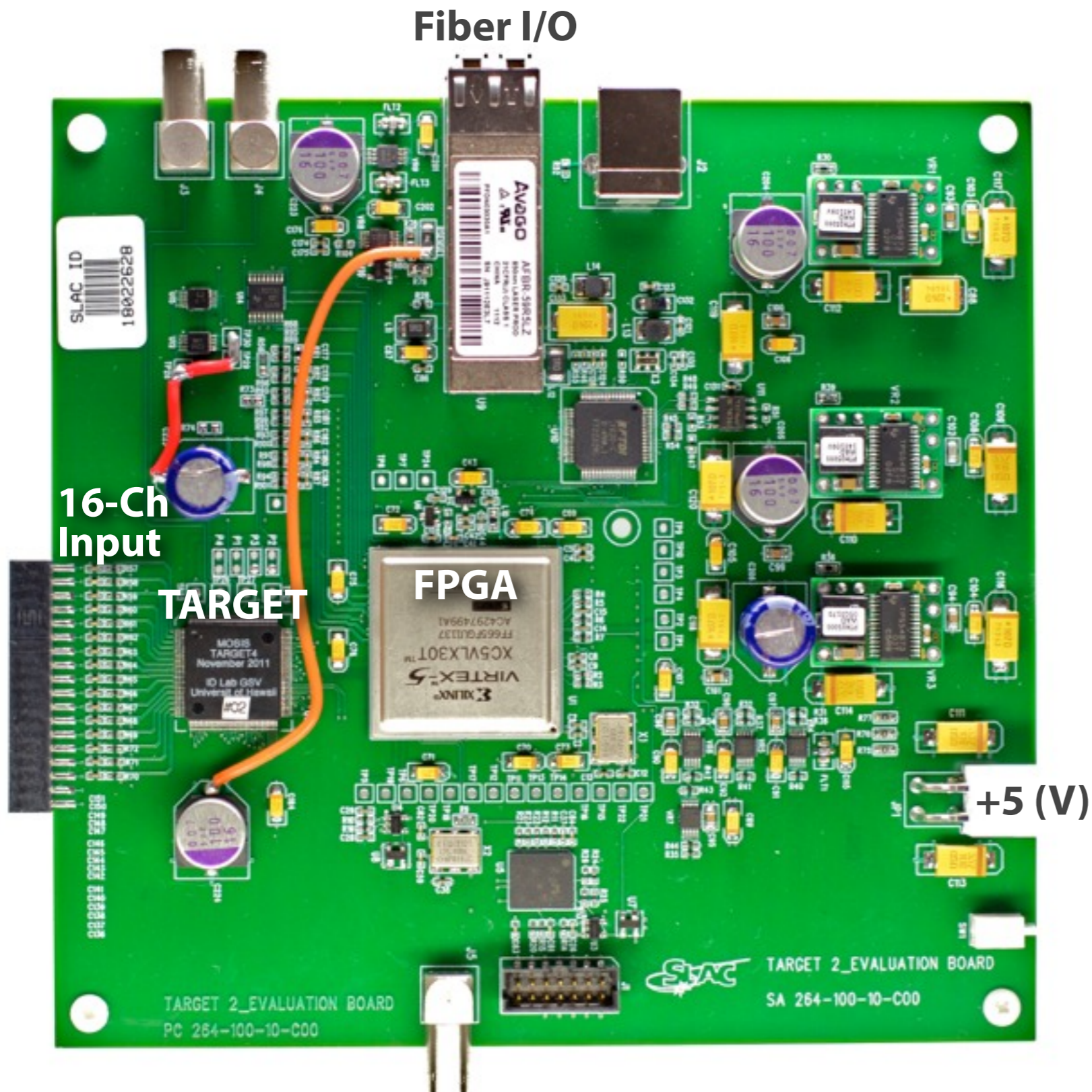
Bechtol+ 2011 (arXiv:1105.1832)

- ❑ Bandwidth is -3 dB @ 150 MHz, not fast enough yet
- ❑ Low slew rate, saturates at V_{pp} of ~ 500 mV
- ❑ To be improved with new TARGET variants

TARGET Variants and Specifications

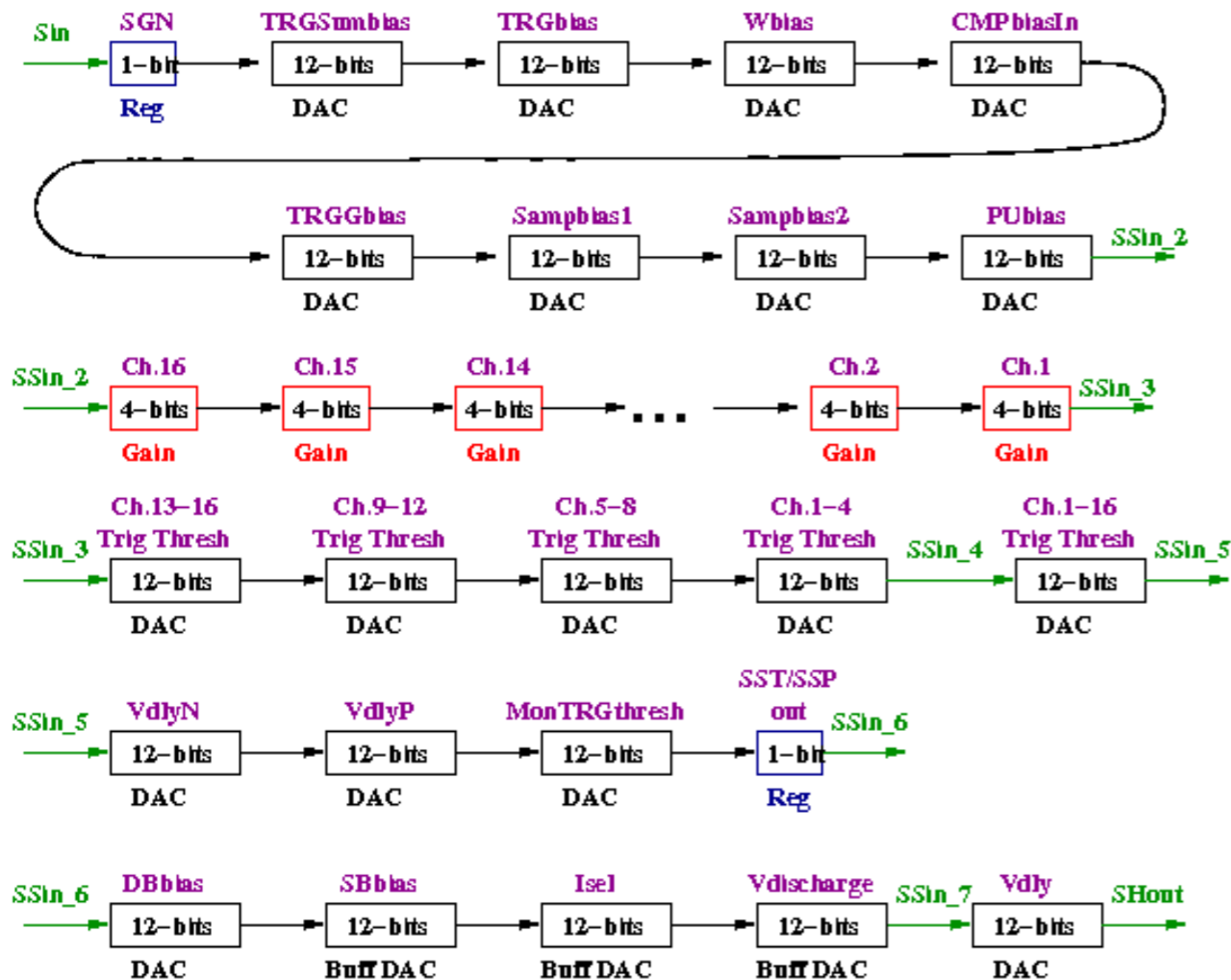
	TARGET 1	TARGET 2	TARGET 3	TARGET 4
Year of Delivery	2010	2011	2011	2012
Number of Channels	16	16	16	16
Storage Cells/Channel	4,096	16,384	16,384	16,384
Sampling Rate (GHz)	0.5 - 2.5	0.5 - 1.5	0.5 - 1.5	0.5 - 1.5
Dynamic Range (Bits)	9	9	10	10
Gain	60	60	none	none
Wilkinson ADC Clock Speed (MHz)	~100	~700	~700	~700
ADC Conversion at a Time (Blocks)	2 × 16	16 × 32	16 × 32	16 × 32
Readout Time per Sample (ns)	20	20	20	20
Trigger Analog Sum		4	none	none
Trigger Outputs	1 + 1	4	4	4
Trigger Thresholds		4 + 1	4 + 1	4 + 1
Trigger Mask		16	16	16
Ramp Offset Adjustment		0 - 1 (V)	0 - 1 (V)	0 - 1 (V)
Ramp Slope Adjustment		0.5 - 10 (μ s)	0.5 - 10 (μ s)	0.5 - 10 (μ s)
PUBias Fast Reset		1	1	1
Improved RCO Monitor		1	1	1

The TARGET-2/3/4 Evaluation Board



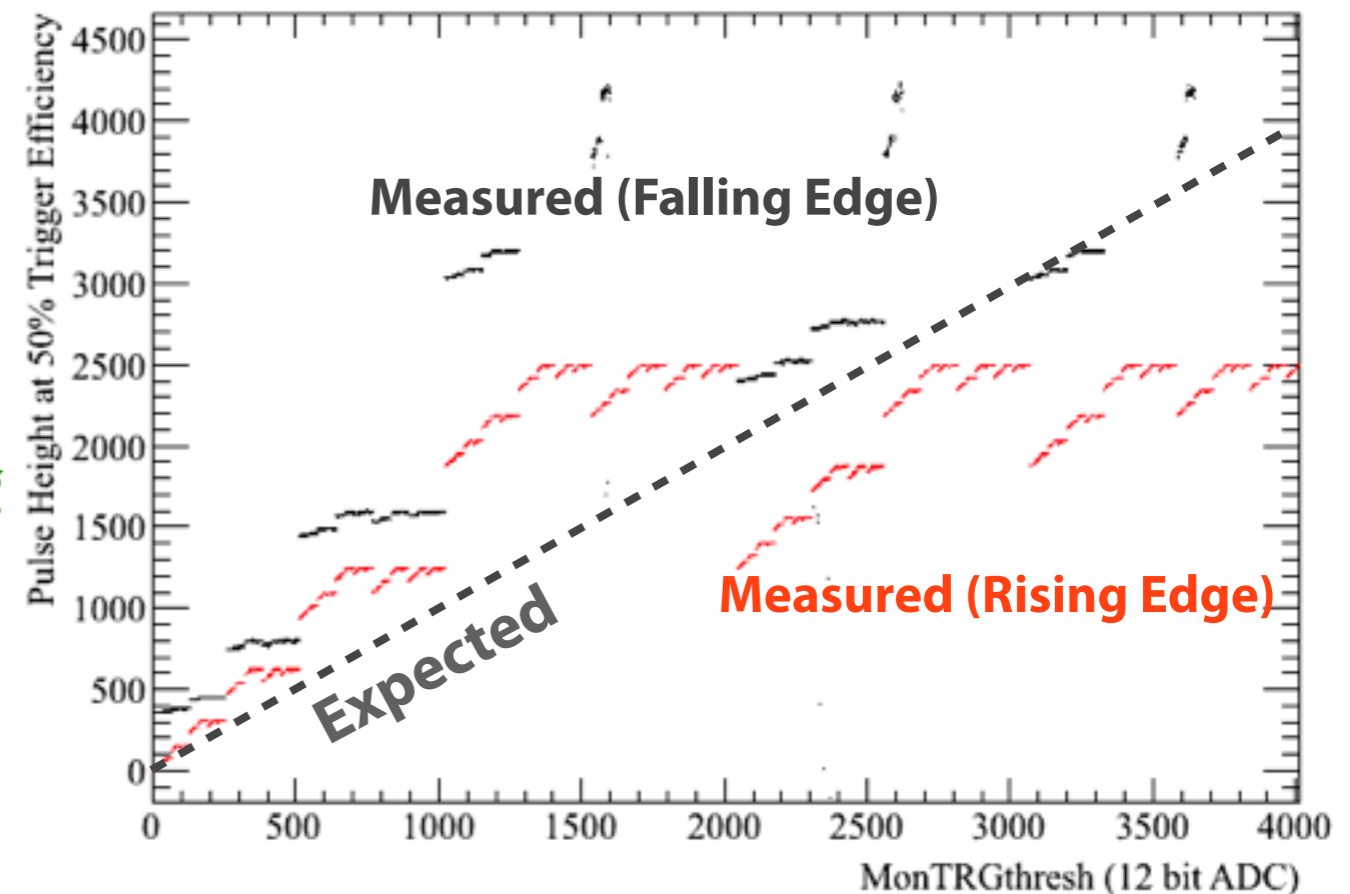
- ❖ Started evaluating TARGET 2 and 3
- ❖ Struggling with some problems which were not observed with TARGET 1
 - ▶ Some control parameters cannot be set properly
 - ▶ A few bias voltages cannot be supplied
 - ▶ Sampling speed is much faster than expected (~2.7 GHz)
 - ▶ “Surgical operation”

Example of "Corrupted" Register Value of TARGET 2



Routing Map of Configuration Register Chain

Measured Threshold



Input Register (Threshold)

- ❑ Configuration register chain sent from FPGA is not properly reflected inside TARGET
- ❑ But essential measurements can be done with limited configuration values
- ❑ Fixed in TARGET 4 (partially)

Summary

- ❖ The **Schwarzschild-Couder telescope** is under development by the CTA-US team + Nagoya University
- ❖ The **prototype camera module** and the **TARGET** ASICs have been developed and being tested
- ❖ New TARGET variants were designed and delivered to improve the TARGET-1 performance
- ❖ Some problems have been found, but we are trying to fix them in 2012